EXPERIMENTAL 9 GBIT/S TRANSMITTER AND RECEIVER FOR OPTICAL TRANSMISSION SYSTEMS

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ABSTRACT

In the trunk network of Deutsche Bundespost Telekom (DBP) optical transmission systems working at 2.4 Gbit/s have been implemented last year. This bitrate could be processed with commercial monolithic integrated GaAs-circuits. For higher bitrates, such as 4.5 Gbit/s or even 9 Gbit/s, monolithic integrated Si-ICs must be applied at the time being. In this paper it is shown that with only a few different types of special Si-ICs all the components for transmission systems working at bitrates of up to 10 Gbit/s can be built up using a sophisticated circuitry.

INTRODUCTION

The transmission systems to be described here are experimental ones with which the optical components like laser diodes, photo diodes, and single mode fibres and also the electronic circuitry shall be tested at bitrates of 4.52 and 9.04 Gbit/s, respectively. Furthermore they are used to demonstrate the quality of systems with high bitrates and to get experiences for a later commercial use. Therefore the bitrates of 4.52 and 9.04 Gbit/s have been chosen independently of any existing standard.

The main task of these transmission systems is to make the high bitrates available for testing, but furthermore it must be possible to insert them into the existing network. Therefore the basic bitrate is 139.264 Mbit/s which e.g. can be one digital TV-channel or one half of a digital HDTV-channel. Fig. 1 shows the block diagram of an existing 4.52 Gbit/s-system, which now is used to generate a first experimental 9.04 Gbit/s-signal by multiplexing its output signal and a 4.52 Gbit/s pseudo random signal.

ASSEMBLY

If bitrates exceed some Gbit/s the design of layout, interconnections, mounting and packaging has to be done under microwave-like conditions. But in contrast to conventional microwave circuits, which normally are rather smallband ones, Gbit/s-circuits need the frequency range from DC to their upper limit. To produce a fairly rectangular appearing puls train, e.g. at 4.5 Gbit/s, at minimum the third harmonic must be included, so that the circuit needs an upper frequency limit of 15 GHz. Therefore all signal interconnections can only be realized as carefully matched microstrip- or coaxial-lines, even for short distances. Because of the same reason high bitrate circuits normally should be used in dice form. But this leeds, on the other hand, to space problems due to the requirement for placing the matching resistors as close as possible around the chip. Additionally every resistor needs its connection to the ground-layer on the rear side of the substrate, which means a lot of metallized through-holes. The best solution of this problem are on-chip terminating resistors. Some of the latest Si-circuits, which can be used for bitrates of up to 10 Gbit/s and more, now have the terminating resistors on the chip.

For bitrates of more than 2 Gbit/s thickfilm ceramic circuits have been found to be suitable for both, encapsulated and unencapsulated circuits, whereas for bitrates of more than 5 or 6 Gbit/s thinfilm circuits show better results. Another possibility are copper-plated ceramic-filled Teflon-substrates. For this 4.5 Gbit/s-system all GaAs-devices have been mounted either on Teflon-substrates or, like the Si-chips, on ceramic thick- or thinfilm-circuits. All interconnection lines and resistors on the mounting side are screen-printed as well as the large areas of decoupling capacitors and power supply layers on the rear. The fastest components are built into microwave packages in order to avoid reflections at the transitions between striplines and coaxial lines, as for instance all parts of the 9 Gbit/s experimental transmitter and receiver, Fig. 2. Moreover, also lower bitrate circuits are realized as thickfilm circuits to get a high packaging density and short signal path lengths for interconnections.

Commercial available monolithic integrated GaAs-ICs have been used for bitrates up to 2.4 Gbit/s which at the moment seems to be the highest bitrate to be handled by these circuits. In addition to reach the 4.5 and 9 Gbit/s we therefore are using monolithic integrated Si-ICs, which have been developed and fabricated by Ruhr-University Bochum and Siemens Munich. The used technology is a standard ECL one with 2 µm dimensions, which partly reaches bitrates up to 7 Gbit/s due to a careful optimization of all components, low internal switching levels and differential signal processing. The new generation of these circuits is produced with 0.8 µm dimensions and increases the available bitrate to more than 10 Gbit/s. In particular the following types of Si-circuits have been used for the transmission systems: Divider, D-flipflop, EXOR, multiplexer, demultiplexer, shift register and clock recovery circuits.

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4.52 GBIT/S TRANSMISSION SYSTEM

The main task of the transmission system is to make the high bitrate available for testing, but furthermore it must be possible to insert it into the existing network. Therefore the basic bitrate is 139.264 Mbit/s which e.g. can be one digital TV-channel or one half of a digital HDTV-channel. Fig. 1 shows the block diagram of the system.

As can be seen, there are three multiplexing steps to reach the 4.5 Gbit/s laser driving signal, starting from 32 input signals of 139 Mbit/s each. These input signals are plesiochronous ones, therefore first they must be made synchronous by a pulse stuffing technique before they can be multiplexed. The synchronous signals have a bit rate of 141.248 Mbit/s and are multiplexed in a first step in groups of four to eight 564.992 Mbit/s signals and in a second step into four 1.13 Gbit/s signals. There is one master-MUX which controls seven slave-MUXs, so that the eight output channels are synchronous and their frame alignment words start at the same time, too. The frame alignment word of the master becomes inverted and serves at the receiving end for synchronization.

Finally, the four 1.13 Gbit/s signals are multiplexed synchronously in a last MUX to the output signal with the bitrate of 4.519934 Gbit/s. With the above mentioned and not scrambled new 24 bit frame alignment word of the master 1.13 Gbit/s channel, appearing at every fourth bit inside the scrambled 4.5 Gbit/s bitstream, a new frame structure is given with a frame length of 21504 bits and a frame alignment word of 96 bits, but only 24 bits of it are used for synchronization.

Laser driver and transimpedance amplifier belong to the optical part of the system. The electronic part at the receiving end begins with a broadband linear amplifier which controls the clock recovery circuit and a combined regenerator and 1:2 demultiplexer. Demultiplexing is done in four steps, from 4.5 Gbit/s to 2 x 2.26 Gbit/s, 4 x 1.13 Gbit/s, 8 x 565 Mbit/s and 32 x 139 Mbit/s. A word frame synchronization circuit is controlled by one of the 1.13 Gbit/s signals and synchronizes the first three demultiplexers, whereas the last DEMUX, which converts the eight 565 Mbit/s signals into the 139 Mbit/s output signals, is self-synchronizing. The 32 output signals are synchronous and can be fed back into the network directly.

The descrambler also is controlled by the word frame synchronization circuit and is started synchronously with respect to the scrambler at the transmitting end. After descrambling the frame alignment word of the master-565 Mbit/s signal becomes reinverted.

9 GBIT/S EXPERIMENTAL TRANSMITTER

For first tests with a 9 Gbit/s signal the simple principle of Fig. 3 was used. The available output signal of the 4.52 Gbit/s transmitter becomes synchronously multiplexed (MUX 2) with a pseudo-random sequence of 4.52 Gbit/s, too, which is the product of multiplexing (MUX 1) two 2.26 Gbit/s pseudo-random signals. These signals have the same pattern, but one of them is delayed by half the number of bits of one full word (in this case the word-length is 127 bit). Therefore the multiplexed pseudo random signal has the same pattern as the lower ones. The differential output signal of the transmitter has an amplitude of 800 mV_{pp} and is the input signal of a laser driver.

Both input signals of MUX 2 are output signals of D-flipflops and for that reason they are nearly free of jitter, which is important because MUX 2 is exclusively built up by gates and therefore no retiming circuit is included. In order to reduce the jitter of its output signal an additional D-flipflop is used for retiming, Fig. 4. The waveform of the 9.04 Gbit/s multiplexer output-signal is shown as the center trace in Fig. 5, the upper trace is one of the two 4.52 Gbit/s input-signals and the lower trace is the 9.04 GHz clock-signal.

9 GBIT/S EXPERIMENTAL RECEIVER

The receiver begins with a buffer amplifier which controls the clock recovery circuit and a D-flipflop, Fig. 6. At the time being, the clock recovery circuit is a passive dielectric-resonator filter in conjunction with two selective amplifiers. Its output frequency is divided by two and drives both, the D-flipflop and the 4.5 Gbit/s-receiver, (the clock recovery circuit of the receiver has been removed). The D-flipflop selects every second bit out of the 9 Gbit/s input-data and therefore its output signal is either corresponding to the information or to the pseudo-random channel at the transmitting side. By means of a synchronization pulse the output signal of the first frequency divider can be inverted to feed the right input signal to the 4.5 Gbit/s receiver.

CONCLUSION

By combining monolithic integrated GaAs- and Si-ICs, DFB-lasers and ternary avalanche photo diodes, it was possible to realize a 4.5 Gbit/s optical transmission system and a first experimental 9 Gbit/s equipment. The current bitrate in the network of DBP of 139.264 Mbit/s was used as input and output base. The 4.5 Gbit/s transmission signal is multiplexed from 32 input signals, a 4 bit scrambler serves as line encoder. The 9 Gbit/s are obtained by multiplexing the 4.52 Gbit/s signal and a pseudo random signal. Hybrid thick- and thinfilm circuits and microwave suited layouts are the necessary requirements for it. As well GaAs-ICs as Si-ICs have been used in order to reach these bitrates at which the Si-ICs are reserved for the highest bitrates.

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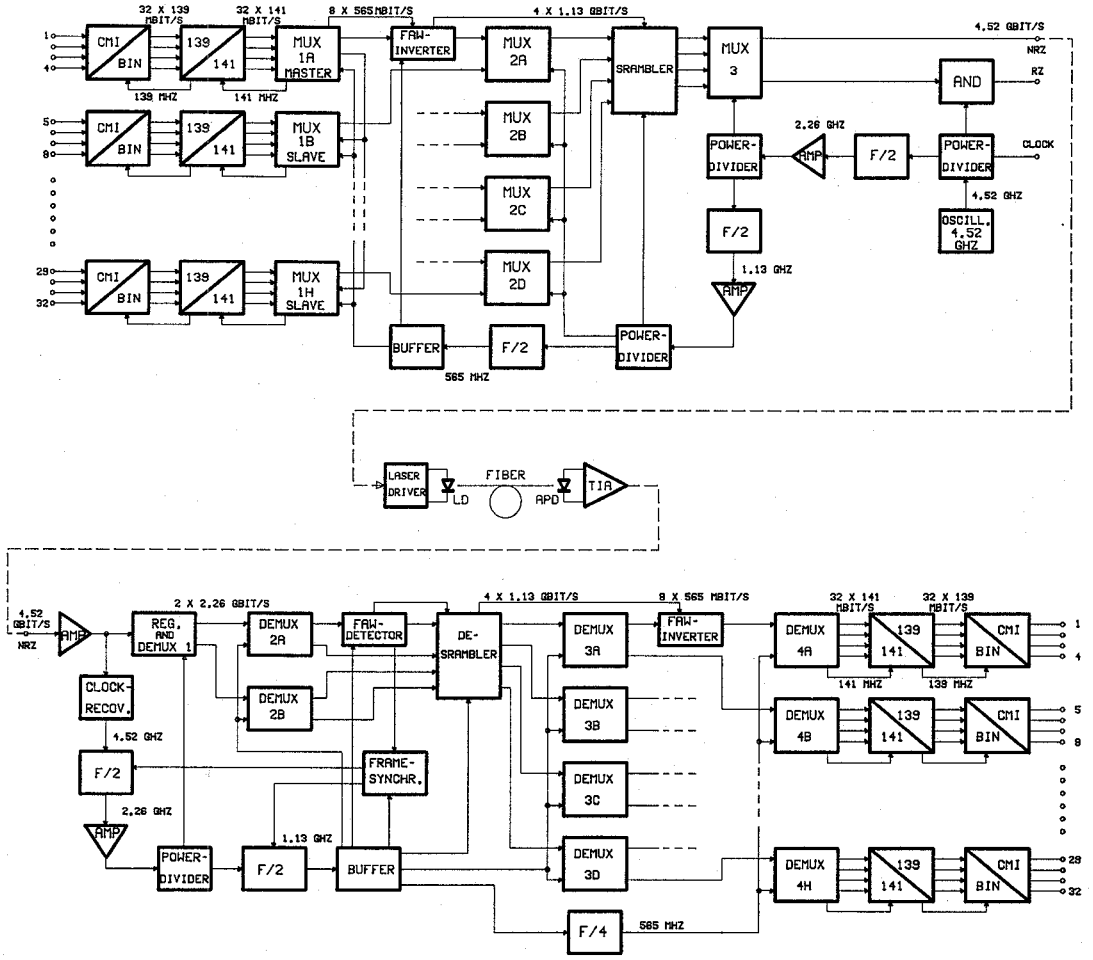

Fig. 1 Block diagram of the optical 4.52 Gbit/s transmission system for 32 plesiochonous 139 Mbit/s input signals.

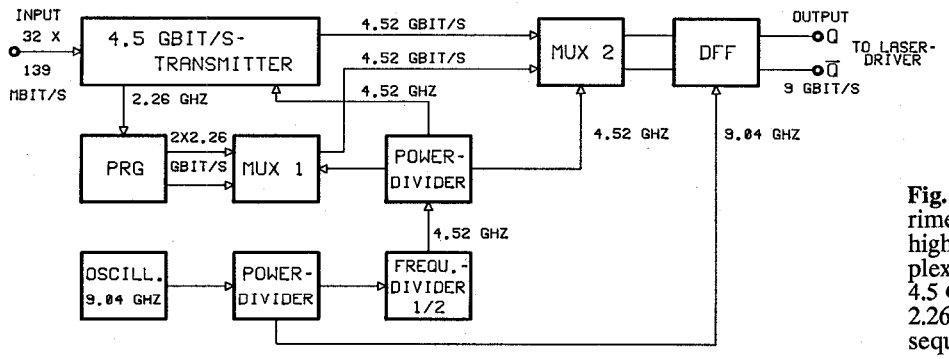

Fig. 3 Principle of the experimental 9 Gbit/s transmitter. The high bitrate is obtained by multiplexing the output signal of the 4.5 Gbit/s system and two 2.26 Gbit/s pseudo random sequences.

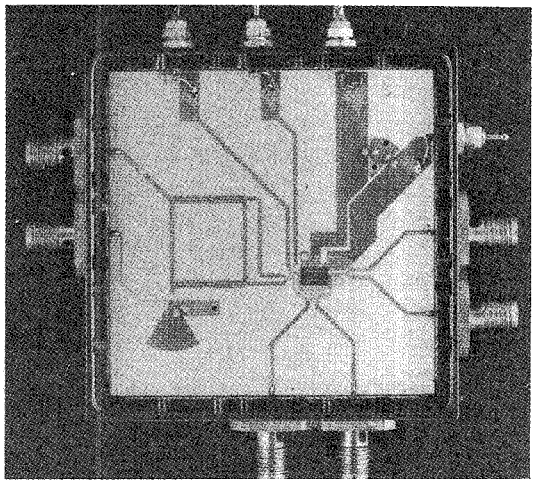

Fig. 2 Example of a thinfilm hybrid circuit, built into a microwave package (pseudo random generator for 3.7 Gbit/s max).

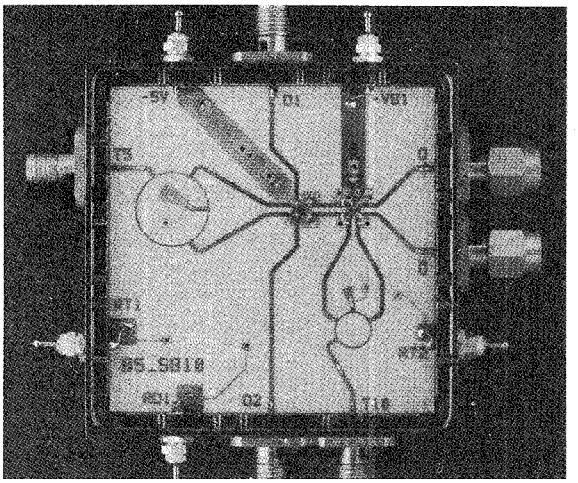

Fig. 4 9 Gbit/s multiplexer module (2:1) as thinfilm microwave integrated circuit, consisting of a MUX-chip and a DFF-chip. The two ring couplers are used for generating the differential 4.5 resp. 9 GHz clock signals.

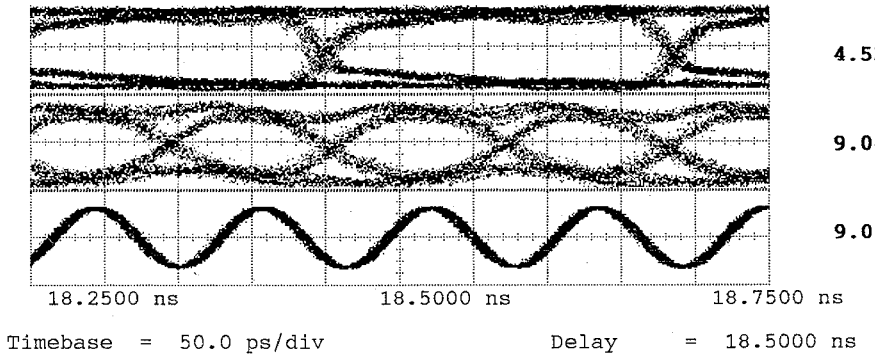

Fig. 5 One of the 4.5 Gbit/s input-signals of the 9 Gbit/s multiplexer (upper trace), 9 Gbit/s output-signal (center trace) and 9 GHz clock-signal.

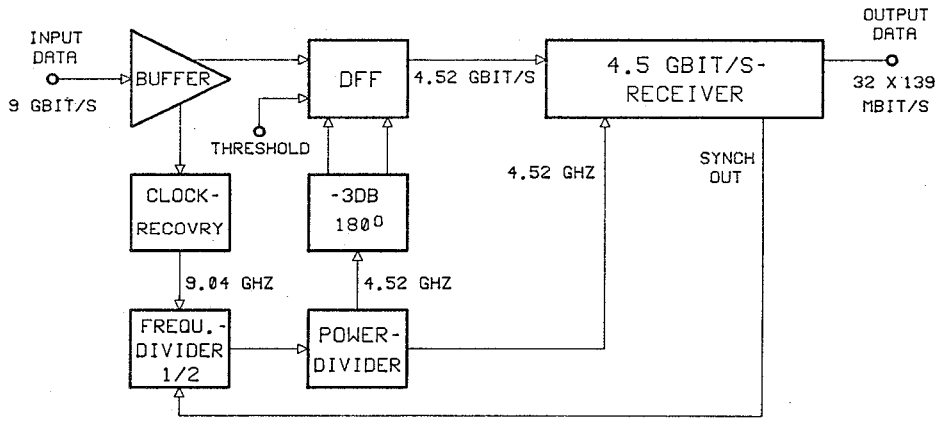

Fig. 6 Principle of the 9 Gbit/s receiver. Only one 4.5 Gbit/s bitstream is demultiplexed out of the 9 Gbit/s input data. Synchronization is done by inverting the 4.5 GHz clock signal.